

## **ABSTRACT**

A system for topology selection to minimize leakage power during synthesis, wherein the system is configured to receive a circuit model that has one or more circuit gates. The system is further configured to receive a library having one or more logic gates, wherein each logic gate has a topology and the leakage sensitivities for each of the topologies is calculated. The system is then configured to synthesize a new circuit model by selecting one or more of the topologies based on its leakage sensitivities, wherein the new circuit model has reduced current leakage.